IC Design Protection in Major Countries

	Statutory Protection	Time Period	Definition
WIPO	TRIPS Agreement: Section 6 Layout-designs of integrated circuits (Article 35)	**10 years** from the date of filing an application for registration or, from the first commercial exploitation wherever in the world it occurs.	"layout-design (topography)" means the three-dimensional disposition, however expressed, of the elements, at least one of which is an active element, and of some or all of the interconnections of an integrated circuit, or such a three-dimensional disposition prepared for an integrated circuit intended for manufacture
TW	Integrated Circuit Layout Protection Act - 1995		A two-dimensional or three-dimensional design of electronic components and interconnecting leads on an integrated circuit
US	17 U.S.C. §§ 901-914 - Enacted through the Semiconductor Chip Protection Act of 1984		Mask work: a series of related images, however fixed or encoded, having or representing the predetermined, three-dimensional pattern of metallic, insulating, or semiconductor material present or removed from the layers of a semiconductor chip product, and in which the relation of the images to one another is such that each image has the pattern of the surface of one form of the semiconductor chip product."
EPO	Council Directive 1987/54/EEC; the Legal Protection of Topographies of Semiconductor Products - 1986		Topography of a semiconductor product: a series of related images, however fixed or encoded - representing the three-dimensional pattern of the layers of which a semiconductor product is composed; - in which series, each image has the pattern or part of the pattern of a surface of the semiconductor product at any stage of its manufacture.
JPN	Act Concerning the Circuit Layout of a Semiconductor Integrated Circuit - 1985		A "circuit layout" in this Act shall mean a layout of circuitry elements and lead wires connecting such elements in a semiconductor integrated circuit.
KR	Semiconductor Integrated Circuits Layout Design Act -1992		"layout design" means a plane or cubic design of the circuit elements and wires that connect the elements that could be used in manufacturing a semiconductor integrated circuit;